AMENDMENTS TO CLAIMS

1. (previously presented) A method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of:

depositing a thin film on the substrate;

depositing a layer of planarizing material on the thin film;

depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material;

depositing a layer of anti-reflective coating on the layer of barrier material;

depositing at least one layer of imaging material on the layer of barrier material;

forming at least one first pattern shape in the layers of imaging material, barrier material, anti-reflective coating and planarizing material;

removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing material;

removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material; and

transferring the first pattern shape to the thin film.

2. (original) The method of Claim 1, wherein at least one second pattern shape is formed in the thin film prior to depositing the layer of planarizing material, and the second pattern shape is filled by the planarizing material.

3. (original) The method of Claim 1, wherein the thin film is a dielectric material.

4. (original) The method of Claim 3, wherein the thin film is a low-k dielectric material.

5. (original) The method of Claim 3, wherein the low-k dielectric material has a dielectric constant less than 3.9.

6. (original) The method of Claim 3, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

7. (original) The method of Claim 1, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and *p*-nitrobenzyl tosylate (pNBT).

8. (original) The method of Claim 1, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

9. (original) The method of Claim 1, wherein the barrier material comprises silicon dioxide deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

10. (original) The method of Claim 9, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

11. (original) The method of Claim 1, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride.

12. (cancelled)

13. (previously presented) The method of Claim 1, further comprising the step of filling the first pattern shape with a conductive material, after removing the imaging material, the barrier material, the anti-reflective coating, and the planarizing material.

14. (original) The method of Claim 13, wherein the conductive material comprises copper.

15. (previously presented) A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:

depositing a dielectric material on the substrate;

forming at least one via in said dielectric material, such that at least one of the vias is positioned over the patterned conductor;

depositing a layer of planarizing material on the dielectric material and in the via;

depositing a layer of barrier material that substantially blocks impurity diffusion from the dielectric material into an imaging material on the layer of planarizing material;

depositing a layer of anti-reflective coating on said barrier material;

depositing at least one layer of imaging material on the layer of barrier material;

forming at least one trench in the layers of imaging material, anti-reflective coating, barrier material and planarizing material, such that at least one of the trenches is positioned over the via;

removing the imaging material, either after or concurrently with forming the trench in the planarizing material;

removing the anti-reflective coating, either after or concurrently with forming the trench in the planarizing material; and

transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via.

16. (original) The method of Claim 15, wherein the dielectric material is a low-k dielectric material.

17. (original) The method of Claim 16, wherein the low-k dielectric material has a dielectric constant less than 3.9.

18. (original) The method of Claim 16, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

19. (original) The method of Claim 16, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

20. (original) The method of Claim 15, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and *p*-nitrobenzyl tosylate (pNBT).

21. (original) The method of Claim 20, further comprising the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material.

22. (original) The method of Claim 20, further comprising the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material.

23. (original) The method of Claim 15, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

24. (original) The method of Claim 15, wherein the barrier material is silicon dioxide.

25. (original) The method of Claim 24, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

26. (original) The method of Claim 24, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

27. (original) The method of Claim 15, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride.

28. (cancelled)

29. (previously presented) The method of Claim 15, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the anti-reflective coating, the barrier material and the planarizing material.

30. (original) The method of Claim 29, wherein the conductive material comprises copper.

31. (original) The method of Claim 15, wherein the at least one via has a height, and the layer of planarizing material has a thickness of about half the via height to about twice the via height.

32. (original) The method of Claim 15, wherein the layer of barrier material has a thickness of about 50 to 100 nm.

33. (previously presented) A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:

depositing a dielectric material on the substrate;

forming at least one trench in the dielectric material, such that at least one of the trenches is positioned over the patterned conductor;

depositing a layer of planarizing material on the dielectric material and in the trench;

depositing a layer of barrier material that substantially blocks impurity diffusion from an underlying interlevel dielectric into an imaging material on the layer of planarizing material;

depositing a layer of anti-reflective coating on said barrier material;

depositing at least one layer of imaging material on the layer of barrier material;

forming at least one via in the layers of imaging material, barrier material and planarizing material, such that at least one of the vias is positioned over the trench and the patterned conductor;

removing the imaging material, either after or concurrently with forming the via in the planarizing material; and

transferring the at least one via to the dielectric material, such that at least one of the vias is positioned over the trench and the patterned conductor;

removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material;

removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material; and,

removing the planarizing material.

34. (original) The method of Claim 33, wherein the dielectric material is a low-k dielectric material.

35. (original) The method of Claim 34, wherein the low-k dielectric material has a dielectric constant less than 3.9.

36. (original) The method of Claim 34, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

37. (original) The method of Claim 34, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

38. (original) The method of Claim 33, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and *p*-nitrobenzyl tosylate (pNBT).

39. (original) The method of Claim 38, further comprising the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material.

40. (original) The method of Claim 33, further comprising the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material.

41. (original) The method of Claim 33, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

42. (original) The method of Claim 33, wherein the barrier material is silicon dioxide.

43. (original) The method of Claim 42, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

44. (original) The method of Claim 42, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

45. (original) The method of Claim 33, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride.

46. (deleted)

47. (previously presented) The method of Claim 33, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the anti-reflective coating, the barrier material and the planarizing material.

48. (original) The method of Claim 47, wherein the conductive material comprises copper.

49. (original) The method of Claim 33, wherein the layer of barrier material has a thickness of about 50 to 100 nm.

50. (previously presented) The method of Claim 1, further comprising the steps of:

removing the barrier layer, either after or concurrently with transferring the first pattern shape to the thin film; and

removing the planarizing material.

51. (previously presented) The method of Claim 15, further comprising the steps of:

removing the barrier material, either after or concurrently with transferring the at least one trench to the dielectric material; and

removing the planarizing material.

52. (previously presented) A method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of:

depositing a thin film on the substrate;

depositing a layer of planarizing material on the thin film;

depositing a barrier material of silicon dioxide on the layer of planarizing material;

depositing at least one layer of imaging material on the silicon dioxide;

forming at least one first pattern shape in the layers of imaging material, silicon dioxide and planarizing material;

removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing material; and

transferring the first pattern shape to the thin film.

53. (previously presented) The method of Claim 52, wherein at least one second pattern shape is formed in the thin film prior to depositing the layer of planarizing material, and the second pattern shape is filled by the planarizing material.

54. (previously presented) The method of Claim 52, wherein the thin film is a dielectric material.

55. (previously presented) The method of Claim 54, wherein the thin film is a low-k dielectric material.

56. (previously presented) The method of Claim 54, wherein the low-k dielectric material has a dielectric constant less than 3.9.

57. (previously presented) The method of Claim 54, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

58. (previously presented) The method of Claim 52, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9 anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6 tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p nitrobenzyl tosylate (pNBT).

59. (previously presented) The method of Claim 52, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

60. (previously presented) The method of Claim 52, wherein the silicon dioxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

61. (previously presented) The method of Claim 60, wherein the silicon dioxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

62. (previously presented) The method of Claim 52, further comprising the steps of:

depositing a layer of anti-reflective coating on the silicon dioxide, prior to depositing the layer of imaging material; and

removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material.

63. (previously presented) The method of Claim 52, further comprising the step of filling the first pattern shape with a conductive material, after removing the imaging material, the silicon dioxide and the planarizing material.

64. (previously presented) The method of Claim 64, wherein the conductive material comprises copper.

65. (previously presented) The method of Claim 52, further comprising the steps of:

removing the silicon dioxide, either after or concurrently with transferring the first pattern shape to the thin film; and

removing the planarizing material.

66. (previously presented) A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:

depositing a dielectric material on the substrate;

forming at least one via in said dielectric material, such that at least one of the

vias is positioned over the patterned conductor;

depositing a layer of planarizing material on the dielectric material and in the via;

depositing a barrier material of silicon dioxide on the layer of planarizing material;

depositing at least one layer of imaging material on the silicon dioxide;

forming at least one trench in the layers of imaging material, silicon dioxide and planarizing material, such that at least one of the trenches is positioned over the via;

removing the imaging material, either after or concurrently with forming the trench in the planarizing material; and

transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via.

67. (previously presented) The method of Claim 66, wherein the dielectric material is a low-k dielectric material.

68. (previously presented) The method of Claim 67, wherein the low-k dielectric material has a dielectric constant less than 3.9.

69. (previously presented) The method of Claim 67, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

70. (previously presented) The method of Claim 67, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

71. (previously presented) The method of Claim 66, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9 anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6 tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p nitrobenzyl tosylate (pNBT).

72. (previously presented) The method of Claim 71, further comprising the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material.

73. (previously presented) The method of Claim 71, further comprising the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material.

74. (previously presented) The method of Claim 66, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

75. (previously presented) The method of Claim 66, wherein the silicon dioxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

76. (previously presented) The method of Claim 66, wherein the silicon dioxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

77. (previously presented) The method of Claim 66, further comprising the steps of:

depositing a layer of anti-reflective coating on the silicon dioxide, prior to deposition of the layer of imaging material; and

removing the anti-reflective coating, either after or concurrently with forming the trench in the planarizing material.

78. (previously presented) The method of Claim 66, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the silicon dioxide, and the planarizing material.

79. (previously presented) The method of Claim 78, wherein the conductive material comprises copper.

80. (previously presented) The method of Claim 66, wherein the at least one via has a height, and the layer of planarizing material has a thickness of about half the via height to about twice the via height.

81. (previously presented) The method of Claim 66, wherein the silicon dioxide has a thickness of about 50 to 100 nm.

82. (previously presented) The method of Claim 66, further comprising the steps of:

removing the silicon dioxide, either after or concurrently with transferring the at least one trench to the dielectric material; and

removing the planarizing material.

83. (previously presented) A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:

depositing a dielectric material on the substrate;

forming at least one trench in the dielectric material, such that at least one of the trenches is positioned over the patterned conductor;

depositing a layer of planarizing material on the dielectric material and in the trench;

depositing a barrier material of silicon dioxide on the layer of planarizing material;

depositing a layer of anti-reflective coating on said barrier material;

depositing at least one layer of imaging material on the layer of barrier material;

forming at least one via in the layers of imaging material, barrier material and planarizing material, such that at least one of the vias is positioned over the trench and the patterned conductor;

removing the imaging material, either after or concurrently with forming the via in the planarizing material; and

transferring the at least one via to the dielectric material, such that at least one of the vias is positioned over the trench and the patterned conductor;

removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material; and

removing the planarizing material.

84. (previously presented) The method of Claim 83, wherein the dielectric material is a low-k dielectric material.

85. (previously presented) The method of Claim 84, wherein the low-k dielectric material has a dielectric constant less than 3.9.

86. (previously presented) The method of Claim 84, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

87. (previously presented) The method of Claim 84, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

88. (previously presented) The method of Claim 83, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9 anthracenylmethylated poly(hydroxystyrene), tetrahydro-1,3,4,6 tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p nitrobenzyl tosylate (pNBT).

89. (previously presented) The method of Claim 88, further comprising the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material.

90. (previously presented) The method of Claim 88, further comprising the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material.

91. (previously presented) The method of Claim 83, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

92. (previously presented) The method of Claim 83, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C.

93. (previously presented) The method of Claim 83, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C.

94. (previously presented) The method of Claim 83, further comprising the steps of:

depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and

removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material.

95. (previously presented) The method of Claim 83, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the barrier material and the planarizing material.

96. (previously presented) The method of Claim 95, wherein the conductive material comprises copper.

97. (previously presented) The method of Claim 83, wherein the layer of barrier material has a thickness of about 50 to 100 nm.